CLAIM AMENDMENTS

Claims 1-22 *(CANCELLED)*

23. *(NEW)* A method for processing electronic data, comprising:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

selectively operating, in response to said first clock signal, on one or more instructions for data processing by

generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions.

24. *(NEW)* The method of claim 23, further comprising generating a status signal indicative of said respective assertion states of said at least one clock control signal.

25. *(NEW)* The method of claim 23, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises logically converting said one or more incoming control signals to said at least one clock control signal.

26. *(NEW)* The method of claim 23, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises storing and reading out said one or more incoming control signals.

27. *(NEW)* The method of claim 23, further comprising generating a second clock signal with active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states.

28. *(NEW)* The method of claim 23, wherein said generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions comprises performing said at least one or more respective portions of one or more decoding operations with decoding circuitry.

29. *(NEW)* The method of claim 23, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded instructions with arithmetic logic circuitry.

30. *(NEW)* The method of claim 23, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises generating said at least one clock control signal with said respective de-assertion states following a second combination of said one or more incoming control signal assertion and de-assertion states.

31. *(NEW)* The method of claim 23, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

32. *(NEW)* The method of claim 23, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

33. *(NEW)* The method of claim 23, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said

one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

34. *(NEW)* The method of claim 23, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

35. *(NEW)* The method of claim 23, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

36. *(NEW)* The method of claim 23, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states

corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

37. *(NEW)* The method of claim 23, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises generating said at least one clock control signal in said respective assertion states following:

said first incoming control signal states combination; and

completion of

said generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions initiated prior to said first incoming control signal states combination, and

said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions.

38. *(NEW)* The method of claim 37, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

39. *(NEW)* The method of claim 37, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a

deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

40. *(NEW)* The method of claim 37, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

41. *(NEW)* The method of claim 37, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

42. *(NEW)* The method of claim 37, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more

incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

43. *(NEW)* The method of claim 37, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

44. *(NEW)* A method for processing electronic data, comprising:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states;

generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively, with said inactive state following said first incoming control signal states combination; and

selectively operating, in response to said first clock signal, on one or more instructions for data processing by

generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more

decoding operations upon each one of at least one or more respective portions of one or more incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions.

45. *(NEW)* The method of claim 44, further comprising generating a status signal indicative of said first clock signal inactive state.

46. *(NEW)* The method of claim 44, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises logically converting said one or more incoming control signals to said at least one clock control signal.

47. *(NEW)* The method of claim 44, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises storing and reading out said one or more incoming control signals.

48. *(NEW)* The method of claim 44, further comprising generating a second clock signal with active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states.

49. *(NEW)* The method of claim 44, wherein said generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions

comprises performing said at least one or more respective portions of one or more decoding operations with decoding circuitry.

50. *(NEW)* The method of claim 44, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded instructions with arithmetic logic circuitry.

51. *(NEW)* The method of claim 44, wherein said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively, comprises generating said at least a first clock signal with said active state following a second combination of said one or more incoming control signal assertion and de-assertion states.

52. *(NEW)* The method of claim 44, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

53. *(NEW)* The method of claim 44, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock

control signal de-assertion and assertion states, respectively.

54. *(NEW)* The method of claim 44, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

55. *(NEW)* The method of claim 44, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

56. *(NEW)* The method of claim 44, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

57. *(NEW)* The method of claim 44, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

58. *(NEW)* The method of claim 44, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises generating said at least one clock control signal in said respective assertion states following:

said first incoming control signal states combination; and

completion of

said generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions initiated prior to said first incoming control signal states combination, and

said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions.

59. *(NEW)* The method of claim 58, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said

generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

60. *(NEW)* The method of claim 58, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

61. *(NEW)* The method of claim 58, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

62. *(NEW)* The method of claim 58, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

63. *(NEW)* The method of claim 58, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

64. *(NEW)* The method of claim 58, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

65. *(NEW)* A method for processing electronic data, comprising:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

generating, in response to said at least one clock control signal, at least a first

clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

selectively operating, in response to said first clock signal, on one or more instructions for data processing by

generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to at least a first one of said plurality of first clock signal cycles, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to at least a second one subsequent to said first one of said plurality of first clock signal cycles, said one or more decoded instructions.

66. *(NEW)* The method of claim 65, further comprising generating a status signal indicative of said respective assertion states of said at least one clock control signal.

67. *(NEW)* The method of claim 65, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises logically converting said one or more incoming control signals to said at least one clock control signal.

68. *(NEW)* The method of claim 65, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises storing and reading out said one or more incoming control signals.

69. *(NEW)* The method of claim 65, further comprising generating a second clock signal with active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states.

70. *(NEW)* The method of claim 65, wherein said generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions comprises performing said at least one or more respective portions of one or more decoding operations with decoding circuitry.

71. *(NEW)* The method of claim 65, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded instructions with arithmetic logic circuitry.

72. *(NEW)* The method of claim 65, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises generating said at least one clock control signal with said respective de-assertion states following a second combination of said one or more incoming control signal assertion and de-assertion states.

73. *(NEW)* The method of claim 65, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states

determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

74. *(NEW)* The method of claim 65, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

75. *(NEW)* The method of claim 65, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

76. *(NEW)* The method of claim 65, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a

plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

77. *(NEW)* The method of claim 65, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

78. *(NEW)* The method of claim 65, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

79. *(NEW)* The method of claim 65, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises generating said at least one clock control signal in said respective assertion states following:

said first incoming control signal states combination; and

completion of

said generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions initiated prior to said first incoming control signal states combination, and

said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions.

80. *(NEW)* The method of claim 79, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

81. *(NEW)* The method of claim 79, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

82. *(NEW)* The method of claim 79, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal,

a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

83. *(NEW)* The method of claim 79, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

84. *(NEW)* The method of claim 79, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

85. *(NEW)* The method of claim 79, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or

more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

86. *(NEW)* A method for processing electronic data, comprising:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states;

generating, in response to said at least one clock control signal, at least a first clock signal having an active state having a plurality of successive cycles and an inactive state having substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively, with said inactive state following said first incoming control signal states combination; and

selectively operating, in response to said first clock signal, on one or more instructions for data processing by

generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to at least a first one of said plurality of first clock signal cycles, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to at least a second one subsequent to said first one of said plurality of first clock signal cycles, said one or more decoded instructions.

87. *(NEW)* The method of claim 86, further comprising generating a status

signal indicative of said first clock signal inactive state.

88. *(NEW)* The method of claim 86, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises logically converting said one or more incoming control signals to said at least one clock control signal.

89. *(NEW)* The method of claim 86, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises storing and reading out said one or more incoming control signals.

90. *(NEW)* The method of claim 86, further comprising generating a second clock signal with active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states.

91. *(NEW)* The method of claim 86, wherein said generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions comprises performing said at least one or more respective portions of one or more decoding operations with decoding circuitry.

92. *(NEW)* The method of claim 86, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded

instructions with arithmetic logic circuitry.

93. *(NEW)* The method of claim 86, wherein said generating, in response to said at least one clock control signal, at least a first clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively, comprises generating said at least a first clock signal with said active state following a second combination of said one or more incoming control signal assertion and de-assertion states.

94. *(NEW)* The method of claim 86, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

95. *(NEW)* The method of claim 86, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

96. *(NEW)* The method of claim 86, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal,

a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

97. *(NEW)* The method of claim 86, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

98. *(NEW)* The method of claim 86, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

99. *(NEW)* The method of claim 86, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or

more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

100. *(NEW)* The method of claim 86, wherein said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises generating said at least one clock control signal in said respective assertion states following:

said first incoming control signal states combination; and

completion of

said generating one or more decoded instructions by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more decoding operations upon each one of at least one or more respective portions of one or more incoming instructions initiated prior to said first incoming control signal states combination, and

said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions.

101. *(NEW)* The method of claim 100, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

102. *(NEW)* The method of claim 100, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

103. *(NEW)* The method of claim 100, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

104. *(NEW)* The method of claim 100, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal and until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

105. *(NEW)* The method of claim 100, further comprising generating, with

data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

106. *(NEW)* The method of claim 100, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, at least a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

107. *(NEW)* A method for processing electronic data, comprising:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states with said respective assertion states following said first incoming control signal states combination;

generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal

having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively; and

executing, with at least a portion of a plurality of subcircuits including pipeline subcircuitry in response to said active second clock signal, one or more instructions for data processing.

108. *(NEW)* The method of claim 107, further comprising generating a status signal indicative of said respective assertion states of said at least one clock control signal.

109. *(NEW)* The method of claim 107, wherein said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises logically converting said one or more incoming control signals to said at least one clock control signal.

110. *(NEW)* The method of claim 107, wherein said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises storing and reading out said one or more incoming control signals.

111. *(NEW)* The method of claim 107, wherein said executing, with at least a portion of a plurality of subcircuits including pipeline subcircuitry in response to said active second clock signal, one or more instructions for data processing comprises decoding said one or more instructions to generate one or more decoded instructions.

112. *(NEW)* The method of claim 111, wherein said executing, with at least a portion of a plurality of subcircuits including pipeline subcircuitry in response to said active second clock signal, one or more instructions for data processing further comprises executing said one or more decoded instructions with arithmetic logic circuitry.

113. *(NEW)* The method of claim 107, wherein said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises generating said at least one clock control signal with said respective de-assertion states following a second combination of said one or more incoming control signal assertion and de-assertion states.

114. *(NEW)* The method of claim 107, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

115. *(NEW)* The method of claim 107, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one

clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

116. *(NEW)* The method of claim 107, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal and until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

117. *(NEW)* The method of claim 107, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal and until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

118. *(NEW)* The method of claim 107, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said second clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more

incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

119. *(NEW)* The method of claim 107, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said second clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

120. *(NEW)* The method of claim 107, wherein said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises generating said at least one clock control signal in said respective assertion states following:

said first incoming control signal states combination; and

completion of said execution of said one or more instructions for data processing initiated prior to said first incoming control signal states combination.

121. *(NEW)* The method of claim 120, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first

clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

122. *(NEW)* The method of claim 120, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

123. *(NEW)* The method of claim 120, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal and until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

124. *(NEW)* The method of claim 120, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal and until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive

states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

125. *(NEW)* The method of claim 120, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said second clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

126. *(NEW)* The method of claim 120, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said second clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

127. *(NEW)* A method for processing electronic data, comprising:

receiving one or more incoming control signals having at least a first combination of respective assertion and de-assertion states corresponding to a power management operation mode;

generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states;

generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively, with said second clock signal inactive state following said first incoming control signal states combination; and

executing, with at least a portion of a plurality of subcircuits including pipeline subcircuitry in response to said active second clock signal, one or more instructions for data processing.

128. *(NEW)* The method of claim 127, further comprising generating a status signal indicative of said second clock signal inactive state.

129. *(NEW)* The method of claim 127, wherein said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises logically converting said one or more incoming control signals to said at least one clock control signal.

130. *(NEW)* The method of claim 127, wherein said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises storing and reading out said one or more incoming control signals.

131. *(NEW)* The method of claim 127, wherein said executing, with at least a portion of a plurality of subcircuits including pipeline subcircuitry in response to said active second clock signal, one or more instructions for data processing comprises decoding said one or more instructions to generate one or more decoded instructions.

132. *(NEW)* The method of claim 131, wherein said executing, with at least a portion of a plurality of subcircuits including pipeline subcircuitry in response to said active second clock signal, one or more instructions for data processing further comprises executing said one or more decoded instructions with arithmetic logic circuitry.

133. *(NEW)* The method of claim 127, wherein said generating, in response to said at least one clock control signal, said first clock signal with active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively, comprises generating said first and second clock signals with said second clock signal active state following a second combination of said one or more incoming control signal assertion and de-assertion states.

134. *(NEW)* The method of claim 127, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-

assertion states.

135. *(NEW)* The method of claim 127, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

136. *(NEW)* The method of claim 127, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal and until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

137. *(NEW)* The method of claim 127, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal and until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states

corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

138. *(NEW)* The method of claim 127, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said second clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

139. *(NEW)* The method of claim 127, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said second clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

140. *(NEW)* The method of claim 127, wherein said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states comprises generating said at least one clock control signal in said respective assertion states following:

said first incoming control signal states combination; and

completion of said execution of said one or more instructions for data processing initiated prior to said first incoming control signal states combination.

141. *(NEW)* The method of claim 140, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

142. *(NEW)* The method of claim 140, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

143. *(NEW)* The method of claim 140, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal and until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or

more incoming control signal assertion and de-assertion states.

144. *(NEW)* The method of claim 140, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said second clock signal and until a reactivation of said second clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.

145. *(NEW)* The method of claim 140, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said second clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more incoming control signals and a first clock signal, at least one clock control signal having respective assertion and de-assertion states related to said one or more incoming control signal assertion and de-assertion states.

146. *(NEW)* The method of claim 140, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said second clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said at least one clock control signal, said first clock signal having active and inactive states substantially independent of said at least one clock control signal assertion and de-

assertion states, and a second clock signal having active and inactive states corresponding to said at least one clock control signal de-assertion and assertion states, respectively.